0.1 Latches and Flip-Flops:

0.1.1 Set Reset Latch (S R Latch) using NOR gate

The circuit diagram of SR latch constructed using NOR gate is as shown in Figure 1

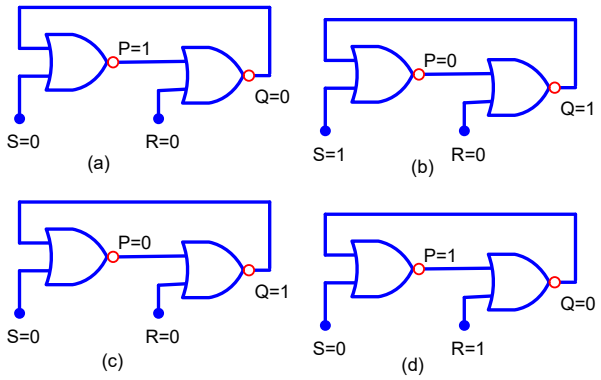

Figure 1

To understand the operation of SR latch made up of NOR gate, first we have to check the truth table of NOR gate.

The output of two input NOR gate is summarized as:

- It's output is 1 when all the inputs are 0.
- Otherwise It's output is 0 if anyone input is 1.

Table 1: NOR gate truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Consider a circuit a diagram of SR latch 1

- In circuit 1(a), when S=0 and R=0: then output Q is 0 if P=1 and then P=1 because S=0 and Q=0. Alternatively when S=0 and R=0: then output Q is 1 if P=0 and then P=0 because S=0 and Q=1. (It's same as the previous content of Q and P)
- In circuit 1(b), When S=1 and R=0: $Q = 1$ and $P = 0$
- In circuit 1(c), When S=0 and R=0: $Q = 1$ and $P = 0$, it maintains its previous state.
- In circuit 1(d), When S=0 and R=1: $Q = 0$ and $P = 1$.
- When S=1 and R=1: When both inputs are 1 then the both the output should be 0 but its not possible, hence it's forbidden input.

Working of S R Latch

- When S=0 and R=0: then output is same as the previous content of Q and $\overline{Q}$
- When S=0 and R=1: $Q = 0$ and $\overline{Q} = 1$
- When S=1 and R=0: $Q = 0$ and $\overline{Q} = 1$
- When S=1 and R=1: When both inputs are 1 then the output should be 0 but its not possible, hence it's forbidden input.

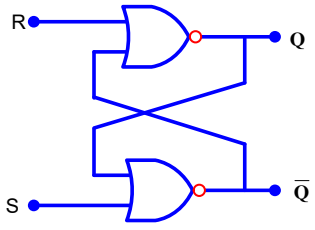

Figure 2

Table 2: SR latch truth table

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	State
0	0	Q	$\overline{Q}$	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	?	?	Forbidden

Table 3: SR latch truth table

S	R	Q_n	Q_{n+1}	State
0	0	0	0	No change
0	0	1	1	No change
0	1	0	0	Reset
0	1	1	0	Reset
1	0	0	1	Set
1	0	1	1	Set
1	1	0	?	Forbidden
1	1	1	?	Forbidden

0.1.2 Set Reset Latch (S R Latch) using NAND gate

The circuit diagram of SR latch constructed using NAND gate is as shown in Figure 3

Table 4: NAND gate truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Working of S R Latch

- When S=0 and R=0: then output is same as the previous content of Q and $\overline{Q}$
- When S=0 and R=1: $Q = 0$ and $\overline{Q} = 1$
- When S=1 and R=0: $Q = 0$ and $\overline{Q} = 1$
- When S=1 and R=1: When both inputs are 1 then the output should be 0 but its not possible, hence it's forbidden input.

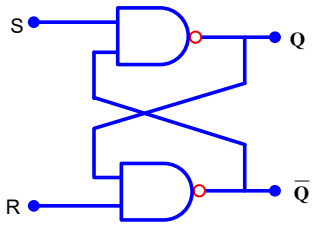

Figure 3

Table 5: SR latch truth table

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	State
0	0	?	?	Forbidden
0	1	0	1	Reset
1	0	1	0	Q is set to 1
1	1	Q	$\overline{Q}$	No change

0.1.3 Gated S R Latch

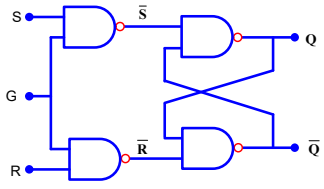

Table 6: SR latch truth table

C	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	State
1	0	0	Q	$\overline{Q}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Q is set to 1
1	1	1	?	?	Forbidden
0	X	X	Q	$\overline{Q}$	No change

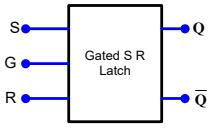

Figure 4

0.1.4 Gated D Latch

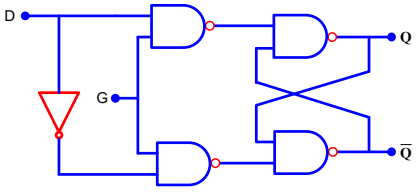

Table 7: SR latch truth table

C	D	Q_{n+1}	$\overline{Q_{n+1}}$
1	0	0	1
1	1	1	0
0	X	Q	$\overline{Q}$

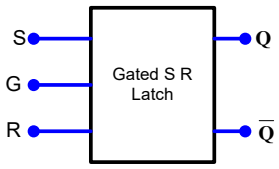

Figure 5

0.1.5 Gated Master Slave SR flip-flop

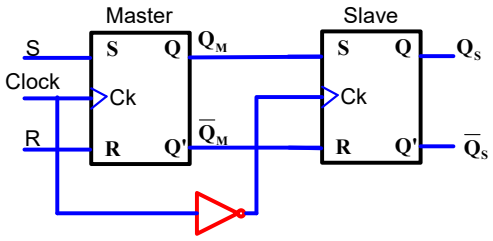

Figure 6: Master Slave SR flip-flop

Table 8: Master Slave SR flip-flop truth table

C	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Status
1	0	0	Q	$\overline{Q}$	No Change
1	0	1	0	1	Set
1	1	0	1	0	Reset
1	1	1	?	?	Forbidden
0	X	X	Q	$\overline{Q}$	No Change

0.1.6 J-K Flip-Flop

The block diagram of J-K Flip-Flop is as shown in Figure 7, which has three inputs J, K and clock. The working principle is similar to the SR flip-flop. The details of the working of J-K Flip-Flop is summarized as:

- When J=0 and K=0 it maintain the content of the previous state.(No change)
- When J=0 and K=1 the flip-flop output is reset to Q = 0 after the active clock edge.
- When J=1 and K=0 the flip-flop output Q is set to Q = 1 after the active clock edge.
- When J=1 and K=1 the flip-flop output Q is change from 0 to 1 or 1 to 0 after the active clock edge.

The detailed truth table and operation of the JK using timing diagram is as shown in Figure.

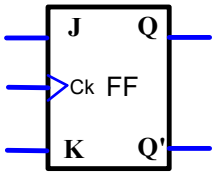

Figure 7: J-K FF

Table 9: Truth table for J K Flip-Flop

J	K	Q	Q_{n+1}	Status
0	0	0	0	No Change
0	0	1	1	No Change
0	1	0	0	Reset
0	1	1	0	Reset
1	0	0	1	Set
1	0	1	1	Set
1	1	0	1	Toggles
1	1	1	0	Toggles

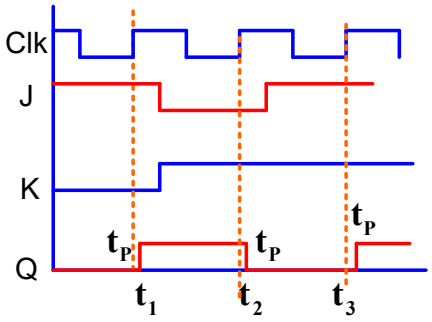

Figure 8: J-K Flip-Flop Timing

$$Q_{n+1} = JQ' + K'Q$$

0.1.7 Edge-Triggered D Flip-Flop

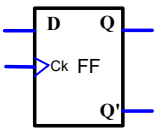

Figure 9: D Flip-Flop

Table 10: D Flip-Flop truth table

C	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Status
1	0	0	Q	$\overline{Q}$	No Change
1	0	1	0	1	Set
1	1	0	1	0	Reset
1	1	1	?	?	Forbidden
0	X	X	Q	$\overline{Q}$	No Change

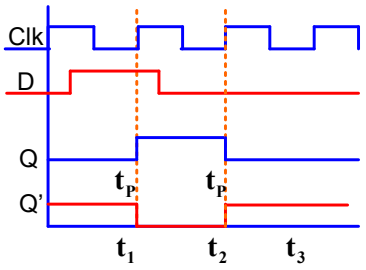

Figure 10: D Flip-Flop Timing

0.1.8 Edge-Triggered T Flip-Flop

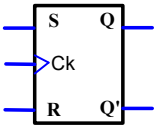

Figure 11: T Flip-Flop

Table 11: D Flip-Flop truth table

C	T	Q	Q_{n+1}	Status
1	0	0	0	No Change
1	0	1	1	No Change
1	1	0	1	Toggle
1	1	1	0	Toggle

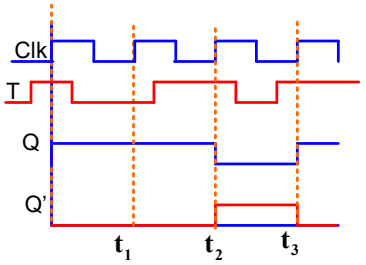

Figure 12: T Flip-Flop Timing

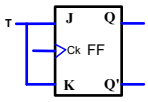

Figure 13: T Flip-Flop

$$Q_{n+1} = T'Q + TQ' = T \oplus Q$$