0.1 Registers:

Flip flops are be used to store a binary data(0 or 1). Each flip flop will store one bit data. To store N number of data N flip flops are used. Registers are memory devices which are made up of flip flops.

The circuit diagram of shift register constructed using D flip flops is as shown in Figure 1. The register has clear(clr) input to clear the content of each flip flop. To load the data into the flip flop, load signal and clock signal are connected through an AND gate. When load=1 the data is applied to each flip flop.

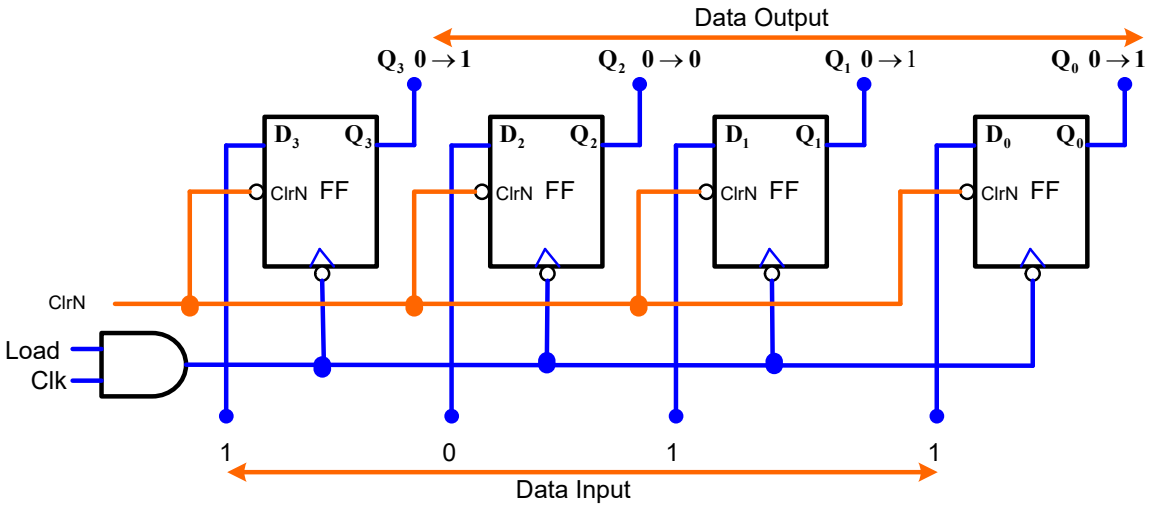


Figure 1

0.2 Shift Register:

Shift Register is a group of flip flops used to store multiple bits of data. There are 4 types Shift registers those are:

1. Serial In Serial Out (SISO)
2. Serial In parallel Out (SIPO)
3. Parallel In Serial Out (PISO)
4. Parallel In parallel Out (PIPO)

4-bit serial-in, serial-out shift register

The circuit diagram of 4 bit Serial In Serial Out (SISO) is as shown in Figure 2. It consists of Serial Input, clock, shift and serial output. When the serial shift is enabled and at the rising edge of the clock data is shifted out. The timing diagram and the shift register output is as shown in Figure 3. The serial data loaded to the shift register is 1 0 0 0 0. The serial input is loaded into the first flip-flop Q3 at the rising edge of the clock. At the same time, the output of the first flip-flop is loaded into the second flip-flop, the output of the second flip-flop is loaded into the third flip-flop, and the output of the third flip-flop is loaded into the last flip-flop.

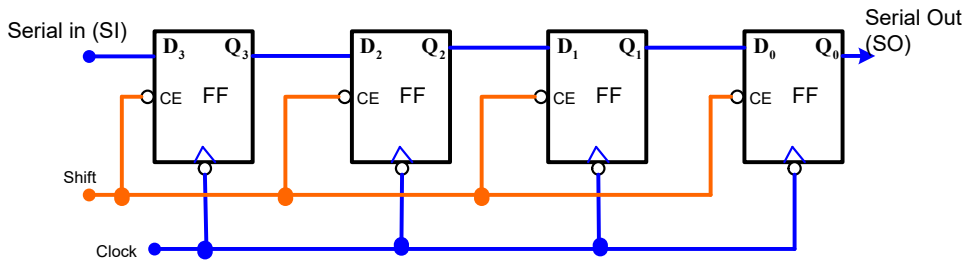


Figure 2

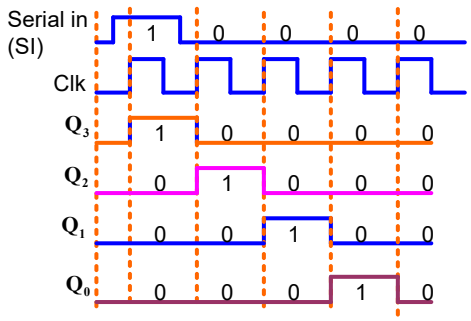


Figure 3

8-bit serial-in, serial-out shift register

The block diagram of 8 bit Serial In Serial Out (SISO) is as shown in Figure 4. The circuit diagram of 8 bit Serial In Serial Out (SISO) is as shown in Figure 5 constructed using SR flipflop. It consists of Serial Input, clock and serial output. At the rising edge of the clock data is shifted out. The timing diagram and the shift register output is as shown in Figure 6. The serial data loaded to the shift register is 0 1 0 1 1 0. The serial input is loaded into the first flip-flop Q7 at the rising edge of the clock. The data 1 and 1 1 will be appear after the 7th clock periods.

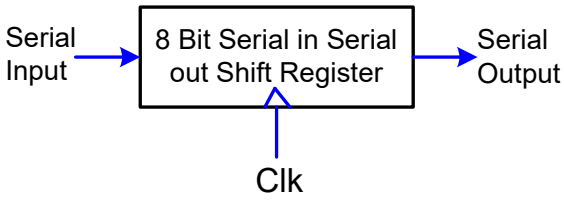


Figure 4

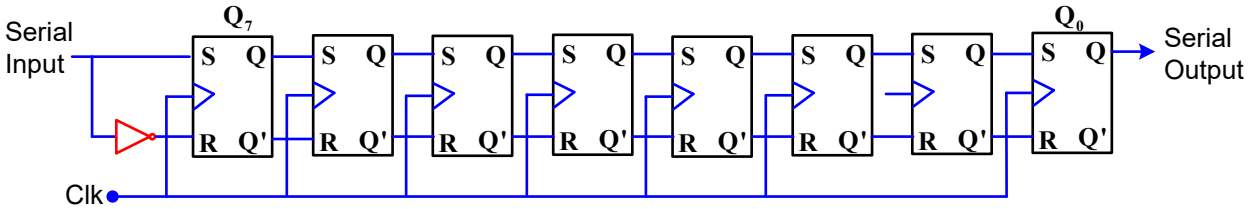


Figure 5

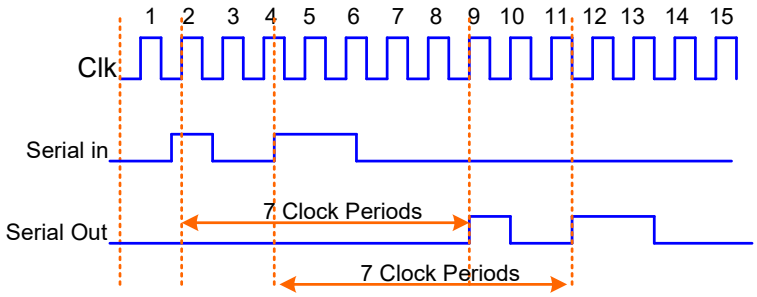


Figure 6

4-bit parallel-in, parallel-out shift register

The block diagram of 4 bit parallel-in, parallel-out (PIPO) is as shown in Figure 7. The circuit diagram of 4 bit parallel-in, parallel-out (PIPO) is as shown in Figure 8 which is constructed using D flipflop. It consists of Parallel Input, clock and Parallel output. At the rising edge of the clock data is shifted out.

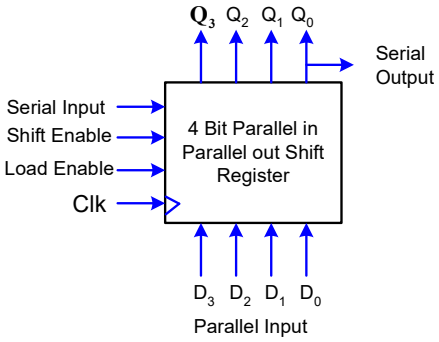


Figure 7

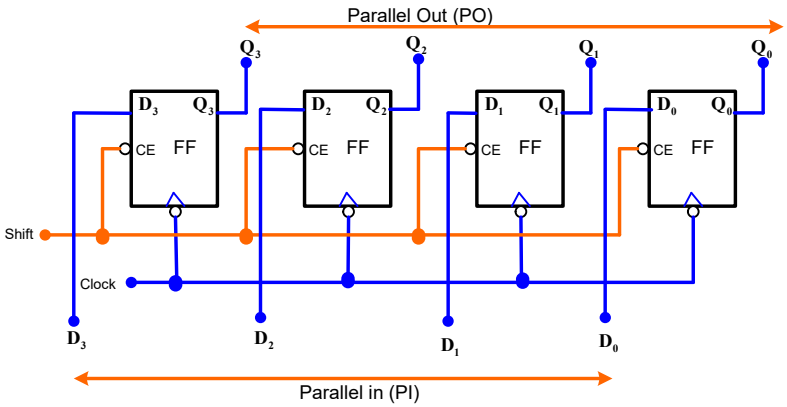


Figure 8

0.3 Counters:

The modulo N synchronous counters counts from 0 to N-1. The synchronous counter uses the same clock signal for all the flip-flops. Counters are constructed using SR flip-flop or JK flip-flop or D flip flop or T flip flop. Synchronous counters use edge-triggered flip-flops and flip-flops will change their state during the next clock pulse.

The following steps are used in designing a synchronous counter.

1. Step 1: No of Flip-Flops required
2. Step 2: Draw the State diagram
3. Step 3: Excitation table based on the type of Flip-Flop
4. Step 4: Obtaining Flip-Flop inputs using K map
5. Step 5: Draw the circuit diagram based on K map equations

Step 1: No of Flip-Flops required:

Binary modulo N counter can count from 0 to N-1. The number of flip flops 'n' required for a modulo N counter is:

$$2^{n-1} <= N <= 2^n$$

For example for mod 5, N=5, number of flip flops 'n' is 3, similarly for mod 12, N=12, number of flip flops 'n' is 4.

The other way of finding the number of flip flops 'n' is

$$n <= log_2 N$$

where n is the number of flip flops and N is modulo count value.

Q1. Design a synchronous 3 bit binary counter using J K flip-flop (sequence 0,1,2,3,4,5,6,7).
OR
Q1. Design a synchronous Mod 8 counter using J K flip-flop (sequence 0,1,2,3,4,5,6,7).

Solution:

Step 1: No of Flip-flops required is

$$2^{n-1} <= N$$
$$2^{3-1} <= 8$$

Hence No of flip-flops required is 3

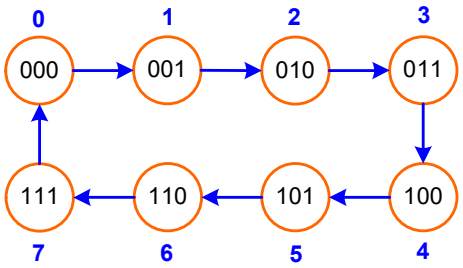


Table 1: J K excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Sl.No	Present State			Next State			Flip flop Inputs					
	Q3	Q2	Q1	Q3	Q2	Q1	J2	K2	J1	K1	J0	K0
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
2	0	1	0	0	1	1	0	X	X	1	1	X
3	0	1	1	1	0	0	1	X	X	1	X	1
4	1	0	0	1	0	1	X	0	0	X	1	X
5	1	0	1	1	1	0	X	0	1	X	X	1
6	1	1	0	1	1	1	X	0	X	0	1	X
7	1	1	1	0	0	0	X	1	X	1	X	1

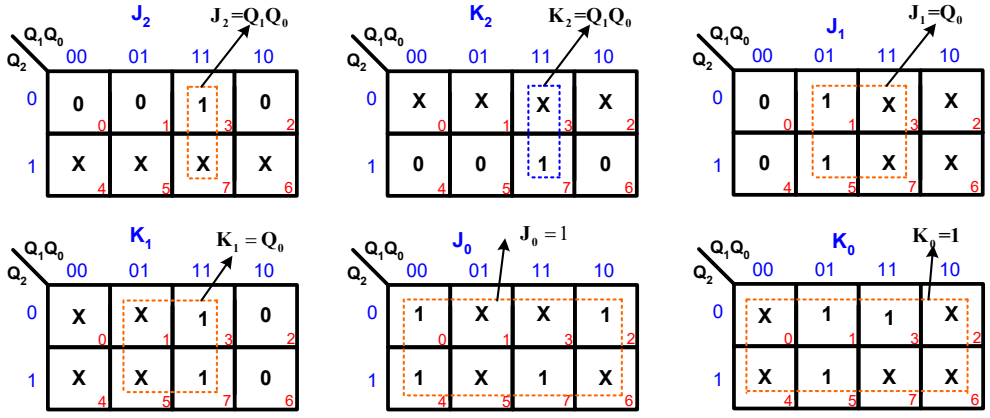


Figure 9

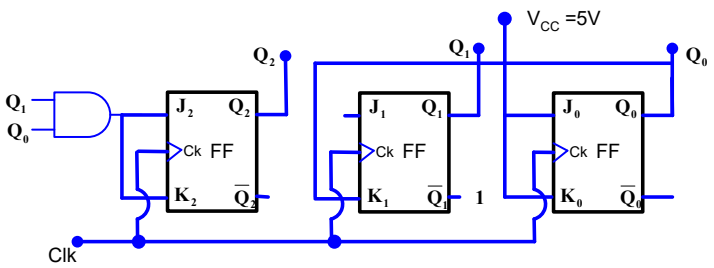


Figure 10

Q1. Design a synchronous 3 bit binary counter using T flip-flop (sequence 0,1,2,3,4,5,6,7).

Solution:

Table 2: T Flip-flop excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Sl.No	Present State			Next State			Flip flop Inputs		
	Q3	Q2	Q1	Q3	Q2	Q1	T3	T2	T1
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	1	1	0	0	1	1
6	1	1	0	1	1	1	0	0	1
7	1	1	1	0	0	0	1	1	1

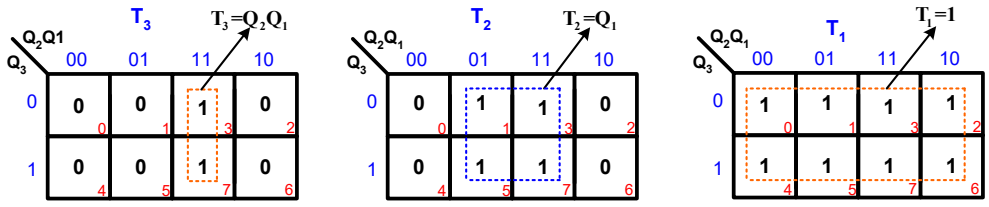


Figure 11

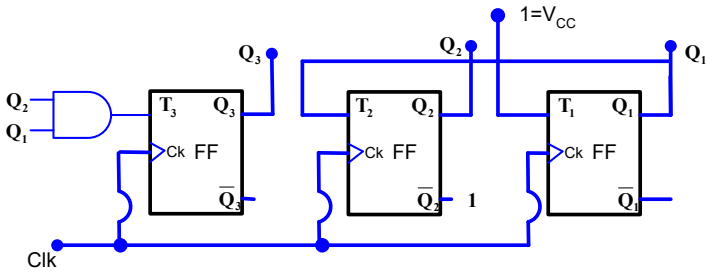


Figure 12

Q1. Design a synchronous counter using J K Flip-flops to count the sequence 0,1,2,4,5,6,0,1,2 use static diagram and state table.

Solution:

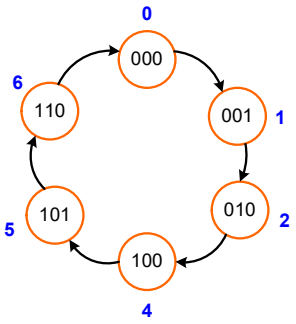


Table 3: J K excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Present State			Next State			Flip flop Inputs					
Q3	Q2	Q1	Q3	Q2	Q1	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
0	1	1	-	-	-	-	-	-	-	-	-
1	1	1	-	-	-	-	-	-	-	-	-

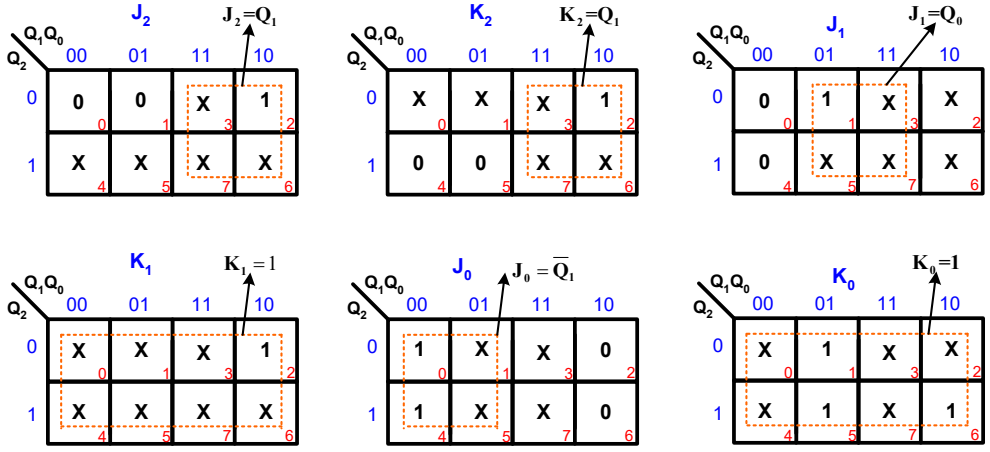


Figure 13

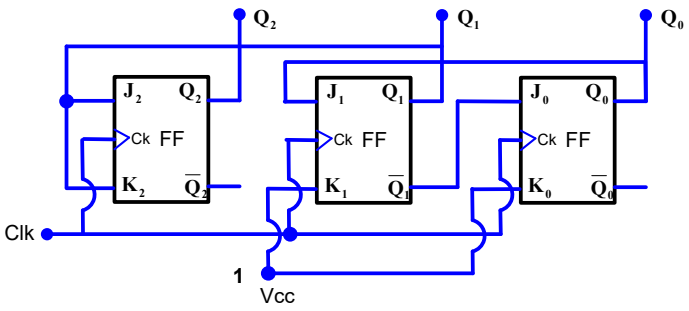


Figure 14

18CSE32 2020-Aug. Design a Mod 5 counter using J K Flip-flops.

Solution:

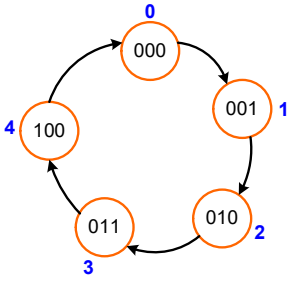


Table 4: J K excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Present State			Next State			Flip flop Inputs					
Q3	Q2	Q1	Q3	Q2	Q1	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	-	-	-	-	-	-	-	-	-
1	1	0	-	-	-	-	-	-	-	-	-
1	1	1	-	-	-	-	-	-	-	-	-

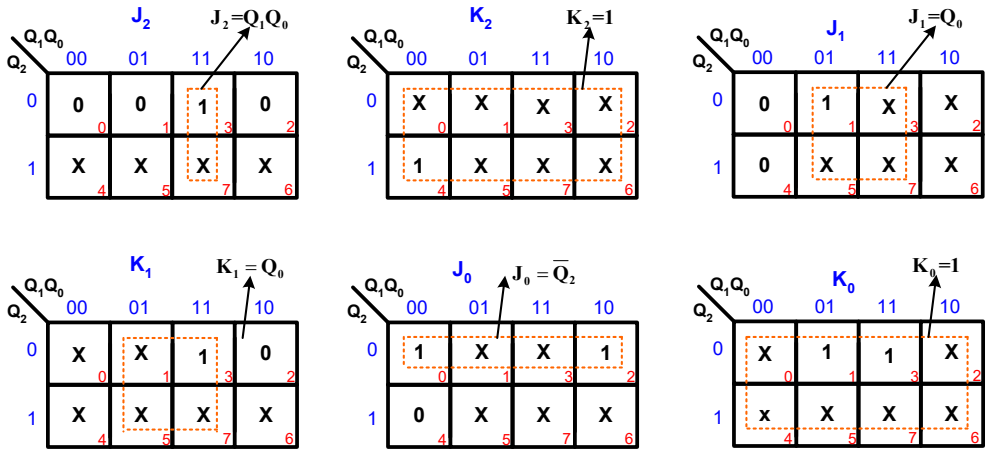


Figure 15

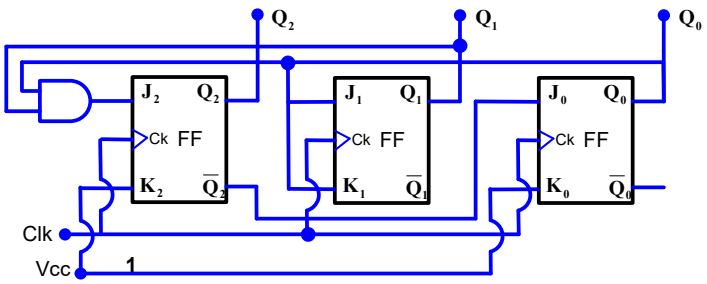


Figure 16

Design a Mod 6 counter using J K Flip-flops.

Solution:

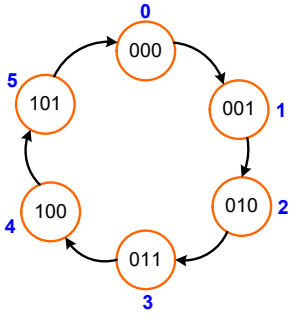


Table 5: J K excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Sl.No	Present State			Next State			Flip flop Inputs					
	Q3	Q2	Q1	Q3	Q2	Q1	J2	K2	J1	K1	J0	K0
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
2	0	1	0	0	1	1	0	X	X	0	1	X
3	0	1	1	1	0	0	1	X	X	1	X	1
4	1	0	0	1	0	1	X	0	0	X	1	X
5	1	0	1	0	0	0	X	1	0	X	X	1
6	1	1	0	X	X	X	X	X	X	X	X	X
7	1	1	1	X	X	X	X	X	X	X	X	X

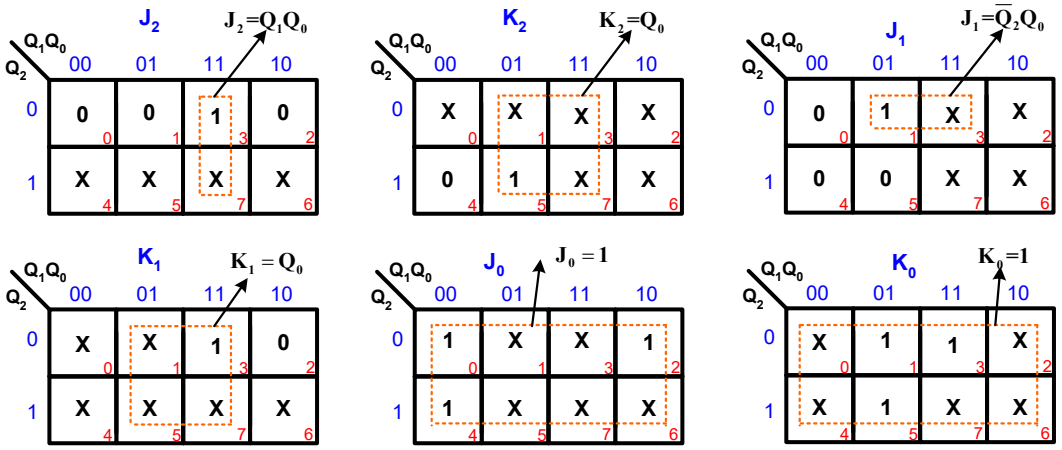


Figure 17

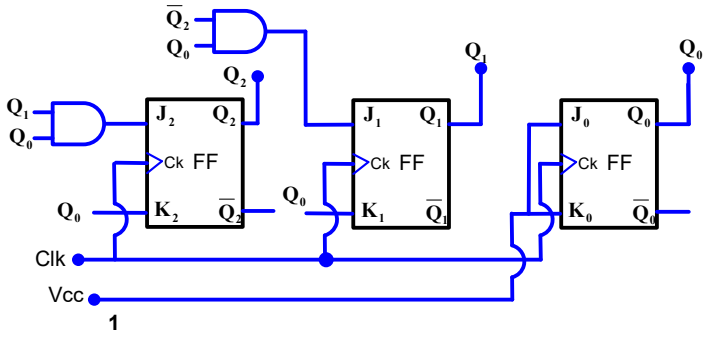


Figure 18

18CSE32 2019-Jan. Design a random counter using T Flip-flops whose transition graph is a shown in Figure.

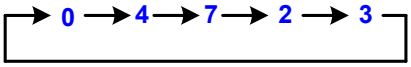


Figure 19

Solution:

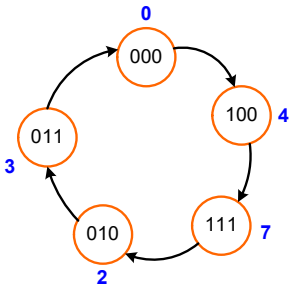


Table 6: T Flip-flop excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Present State			Next State			Flip flop Inputs		
Q3	Q2	Q1	Q3	Q2	Q1	T3	T2	T1
0	0	0	1	0	0	1	0	0
0	0	1	-	-	-	-	-	-
0	1	0	0	1	1	0	0	1
0	1	1	0	0	0	0	1	1
1	0	0	1	1	1	0	1	1
1	0	1	-	-	-	-	-	-
1	1	0	-	-	-	-	-	-
1	1	1	0	1	0	1	0	1

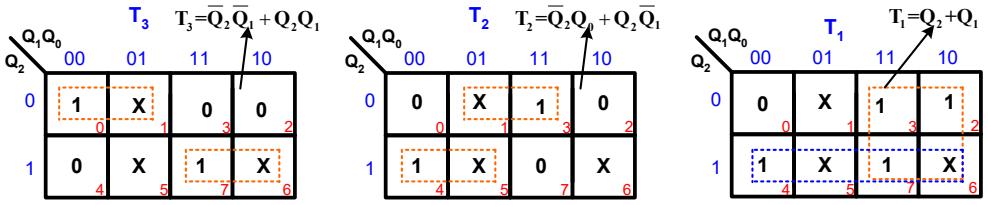


Figure 20

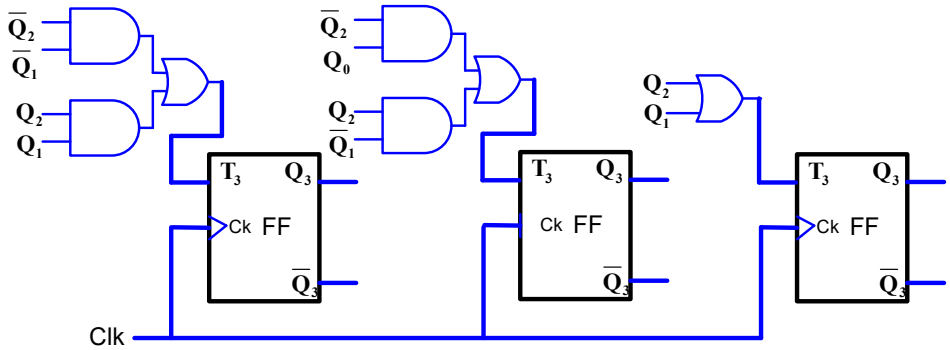


Figure 21

Design a random counter using S R Flip-flops whose transition graph is a shown in Figure.

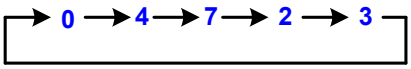


Figure 22

Solution:

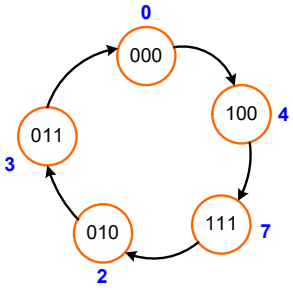
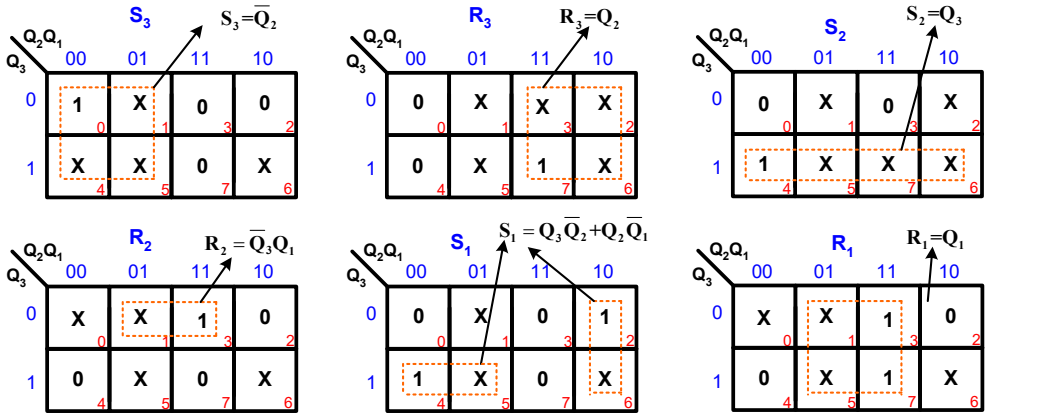


Table 7: S R Flip-flop excitation table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Sl.No	Present State			Next State			Flip flop Inputs					
	Q3	Q2	Q1	Q3	Q2	Q1	S3	R3	S2	R2	S1	R1
0	0	0	0	1	0	0	1	0	0	X	0	X
1	0	0	1	-	-	-	X	X	X	X	X	X
2	0	1	0	0	1	1	0	X	X	0	1	0
3	0	1	1	0	0	0	0	X	0	1	0	1
4	1	0	0	1	1	1	X	0	1	0	1	0
5	1	0	1	-	-	-	X	X	X	X	X	X
6	1	1	0	-	-	-	X	X	X	X	X	X
7	1	1	1	0	1	0	0	1	X	0	0	1



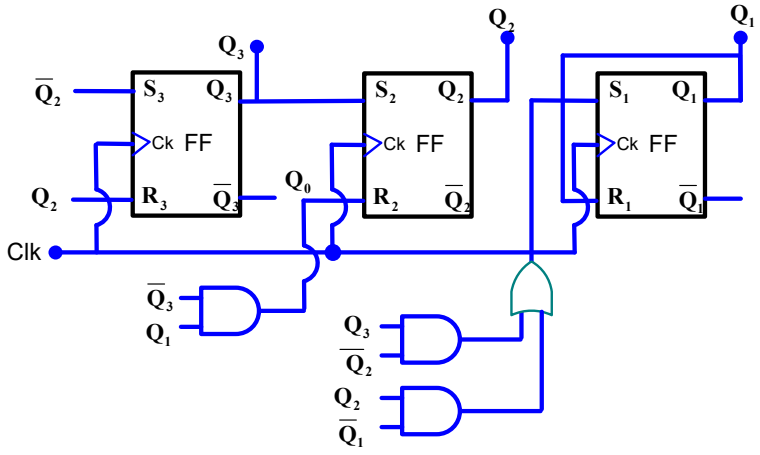


Figure 23

18EC32 2012-June. Design a synchronous counter using J-K flip-flops whose sequence 0-1-4-6-7-5-0... by obtaining minimal sum equations.

Solution:

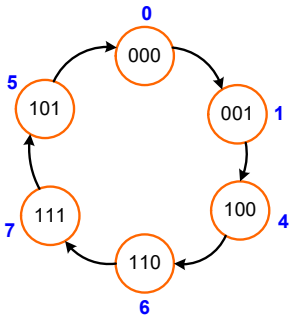


Table 8: J K excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Sl.No	Present State			Next State			Flip flop Inputs					
	Q3	Q2	Q1	Q3	Q2	Q1	J2	K2	J1	K1	J0	K0
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	1	0	0	1	X	0	X	X	1
2	0	1	0	X	X	X	X	X	X	X	X	X
3	0	1	1	-	-	-	X	X	X	X	X	X
4	1	0	0	1	1	0	X	0	1	X	0	X
5	1	0	1	0	0	0	X	1	0	X	X	1
6	1	1	0	1	1	1	X	0	X	0	1	X
7	1	1	1	1	0	1	X	0	X	1	X	0

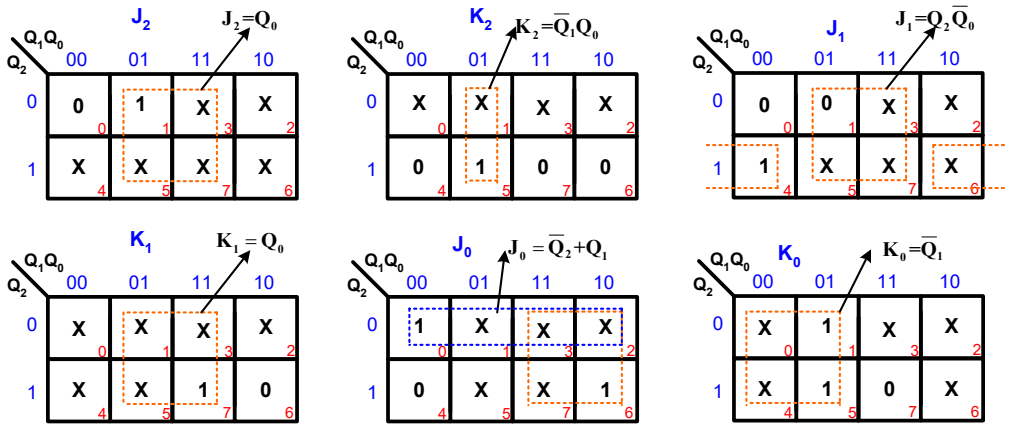


Figure 24

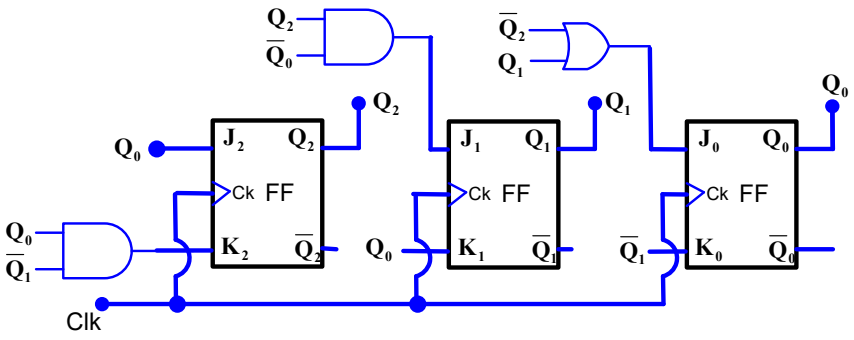


Figure 25

Self Starting Counter: When a power is switched ON if it enters into an invalid or unused state then the condition is called lock-in condition. A counter is said to be self starting, if it can come back to any of the valid counting state after entering into an invalid or unused state is called Self Starting Counter.

Q. Design a self correcting synchronous mod 6 counter using J-K flip-flops.

Solution:

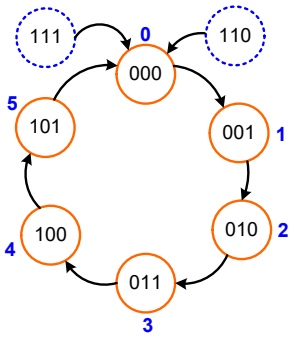
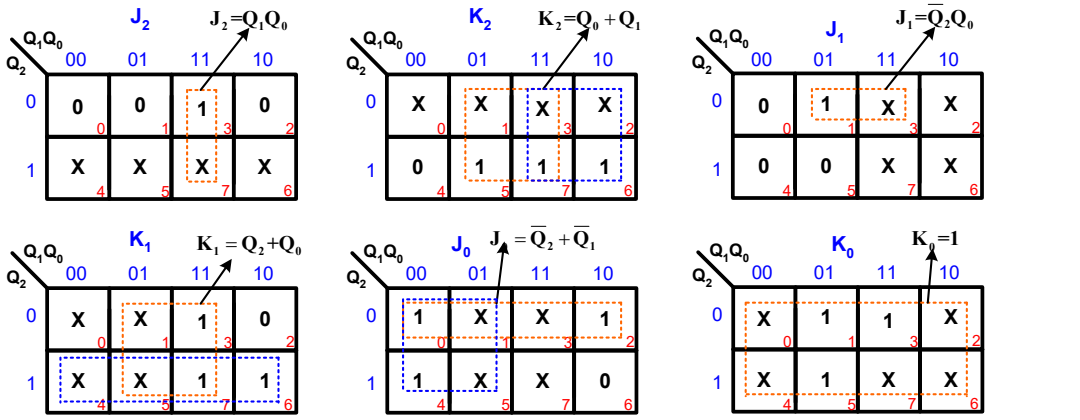


Table 9: J K excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Sl.No	Present State			Next State			Flip flop Inputs					
	Q3	Q2	Q1	Q3	Q2	Q1	J2	K2	J1	K1	J0	K0
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
2	0	1	0	0	1	1	0	X	X	0	1	X
3	0	1	1	1	0	0	1	X	X	1	X	1
4	1	0	0	1	0	1	X	0	0	X	1	X
5	1	0	1	0	0	0	X	1	0	X	X	1
6	1	1	0	0	0	0	X	1	X	1	0	X
7	1	1	1	0	0	0	X	1	X	1	X	1



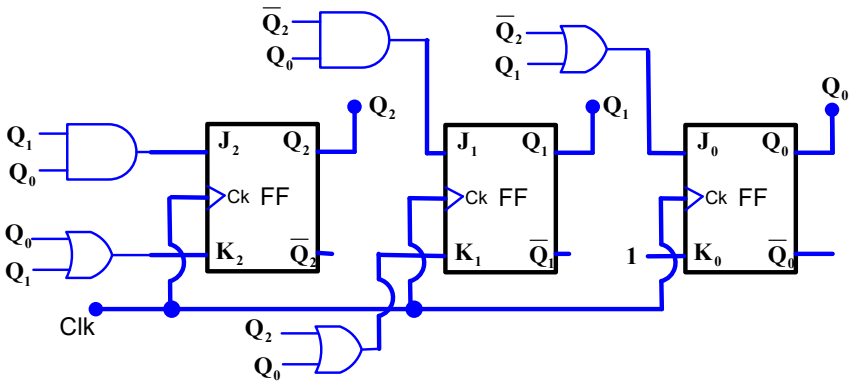


Figure 26